WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

a memory array organized in pages of a first width, which memory array is addressable as pages of the first width and addressable as pages of a second width that is an additional width greater than the first width;

wherein, when addressable as pages of the second width, the additional width of each page of the second width is mapped into at least one associated page of the first width.

2. The invention defined in claim 1 wherein:

when addressed as pages of the second width, each respective page is addressable as a respective basic page of the first width and as a respective extended page of a width smaller than the first width.

3. The invention defined in claim 2 wherein:

when addressed as pages of the second width, the memory array is configured to map each extended page into a corresponding portion of a corresponding basic page.

4. The invention defined in claim 1 wherein:

the memory array, when first addressed as pages of the second width, is configured to map the additional width of each respective page of the second width into a respective associated page of the first width.

5. The invention defined in claim 1 wherein:

the memory array comprises a non-volatile memory array.

6. The invention defined in claim 5 wherein:

the memory array comprises a non-volatile memory array.

7. The invention defined in claim 1 wherein:

the non-volatile memory array comprises passive element memory cells.

8. An integrated circuit comprising:

a memory array organized as a plurality of pages having a page width;

an address translation block for translating an address of an effective location within a page that falls beyond the page width, into a corresponding address of a corresponding location of a corresponding page that falls within the page width, thereby mapping an effective page location beyond its page width into an associated page.

9. The invention defined in claim 8 wherein:

the address translation block is arranged to map at least one address bit that specifies a page into an address bit specifying a location within an associated page.

10. The invention defined in claim 8 wherein:

the address translation block is arranged to map effective locations within the pages beyond the page width into a contiguous group of pages located at one end of the memory array.

11. The invention defined in claim 8 wherein:

the page width is equal to a first integral power of two; and

the number of mapped locations of each page is equal to a second integral power of two.

12. The invention defined in claim 11 wherein:

the first integral power of two is not equal to the second integral power of two.

13. The invention defined in claim 8 wherein:

the memory array comprises a non-volatile memory array.

14. The invention defined in claim 8 wherein:

the memory array comprises a plurality of sub-arrays.

15. The invention defined in claim 8 wherein:

the memory array comprises at least one sub-array, each of which includes a plurality of memory cells, each coupled to a respective one of a plurality of first array terminal lines and coupled to a respective one of a plurality of second array terminal lines; and

the first page width is smaller than the number of memory cells respectively coupled to each of the plurality of first array terminal lines.

16. The invention defined in claim 8 wherein:

the memory array comprises at least one sub-array, each of which includes a plurality of memory cells, each coupled to a respective one of a plurality of first array terminal lines and coupled to a respective one of a plurality of second array terminal lines; and

the first page width is greater than or equal to the number of memory cells respectively coupled to each of the plurality of first array terminal lines.

17. An integrated circuit comprising:

a memory array organized as a plurality of at least 2^D pages, each of width 2^W; and

an address translation block for translating an address that references an effective location within a page that is greater than its page width 2^W by up to an additional width 2^X, into a corresponding address that references a corresponding location within a corresponding page of width 2^W;

wherein D, W, and X are non-negative integers, W is greater than X, and D is greater than (W – X).

18. The invention defined in claim 17 wherein:

the memory array is addressable as at least $2^D - 2^{D-(W-X)}$ pages of width $2^W + 2^X$, each such page comprising a basic page of width 2^W and an extended page of width 2^X; and

the address translation block is configured to map the 2^D extended pages of width 2^X into a group of $2^{D-(W-X)}$ basic pages of width 2^W.

19. The invention defined in claim 18 wherein:
the group of $2^{D-(W-X)}$ basic pages into which the extended pages are mapped are contiguous pages located at one end of the memory array.

20. The invention defined in claim 19 wherein:
the respective extended pages of a plurality of adjacent pages are mapped into a single basic page.

21. The invention defined in claim 19 wherein:
the memory array comprises a non-volatile memory array.

22. The invention defined in claim 18 wherein:
the group of $2^{D-(W-X)}$ basic pages into which the extended pages are mapped are non-contiguous pages comprising at least two groups of at least one page per group within the memory array.

23. The invention defined in claim 18 wherein:
X is within the range 3 to 5; and
W is within the range 6 to 12.

24. The invention defined in claim 17 wherein:
the memory array comprises a non-volatile memory array of passive element memory cells.

25. The invention defined in claim 17 wherein:
the memory array comprises a plurality of sub-arrays.

26. The invention defined in claim 17 wherein:
each page location comprises a plurality of memory cells.

27. The invention defined in claim 26 wherein:
the plurality of memory cells comprising each page location are distributed among at least two sub-arrays.

28. The invention defined in claim 26 wherein:

the plurality of memory cells comprising each page location are disposed in a single sub-array.

29. An integrated circuit comprising:

a memory array having at least 2^M rows and having 2^N columns of memory locations, but which is addressable as rows having more than 2^N columns;

wherein a location having a column address greater than 2^N is mapped into an associated location of an associated row, having a column address no larger than 2^N; and

wherein M and N positive integers.

30. The invention defined in claim 29 further comprising:

an address translation block for translating an address having a row address portion up to 2^M and having a column address portion greater than 2^N by up to an additional 2^X, into a corresponding address having a corresponding row address portion and having a corresponding column address portion no greater than 2^N.

31. The invention defined in claim 30 wherein:

the memory array is addressable as at least $2^M - 2^{M-(N-X)}$ rows, each having $2^N + 2^X$, columns; and

the address translation block is configured to map the upper 2^X addressable columns of each of the 2^M rows into a group of $2^{M-(N-X)}$ rows each having 2^N columns.

32. The invention defined in claim 31 wherein:

the group of $2^{M-(N-X)}$ rows into which the upper 2^X addressable columns are mapped are contiguous rows located at one end of the memory array.

33. The invention defined in claim 31 wherein:

the group of $2^{M-(N-X)}$ rows into which the upper 2^X addressable columns are mapped are non-contiguous rows comprising at least two groups of at least one row per group within the memory array.

34. The invention defined in claim 31 wherein:
X is within the range 3 to 5; and
N is within the range 6 to 12.

35. The invention defined in claim 29 wherein:
the memory array comprises a non-volatile memory array.

36. The invention defined in claim 29 wherein:
the memory array comprises a plurality of sub-arrays.

37. The invention defined in claim 29 wherein:
each memory location comprises a plurality of memory cells distributed among at least two memory sub-arrays.

38. An integrated circuit comprising:
a memory array addressable as a plurality P1 of pages of a width S1 defining a corresponding number of bits N1, and also addressable as a plurality P2 of pages of a width S2 defining a corresponding number of bits N2;
wherein P1 is not equal to P2, and S1 is not equal to S2.

39. The invention defined in claim 38 wherein:
N1 substantially equals N2.

40. The invention defined in claim 38 wherein:
S1 is an integral power of two;
S2 is not an integral power of two; and
S2 is larger than S1.

41. The invention defined in claim 40 wherein:
(S2 – S1) is an integral power of two.

42. The invention defined in claim 40 wherein:
S1 is equal to 512; and
S2 is equal to 528.

43. The invention defined in claim 40 wherein:
the memory is configured to be addressable only as page width S2 when such larger page width is first addressed.

44. The invention defined in claim 38 wherein:
the memory comprises a plurality of non-volatile memory sub-arrays; and
the memory is configured to store more than one bit at each page location.

45. An integrated circuit comprising:
a memory array of memory cells organized in pages, which memory array is addressable in a first mode as pages of a first width and addressable in a second mode as pages of a second width different than the first width;
wherein substantially every memory cell that is addressable in one of the first and second modes is also addressable in the other mode.

46. The invention defined in claim 45 wherein:
at least one of the first width and second width is not an integral power of two.

47. An integrated circuit comprising:
a memory array having at least a number R of rows and having at least a number C of columns of memory locations, having at least some dually-addressable memory locations, each said dually-addressable memory location being addressable at a respective first row address and respective first column address, and also addressable at a respective second row address and respective second column address;
wherein the respective first row address is different than the respective second row address, and the respective first column address is different than the respective second column address, for at least one dually-addressable memory location.

48. The invention defined in claim 47 wherein:
each dually-addressable memory location, once any of such locations is addressed at its respective second row address and respective second

column address, is configured to only be addressable at its respective second row address and respective second column address.

49. The invention defined in claim 48 wherein:
the memory array comprises non-volatile passive element memory cells.

PTO/SB/21 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE